The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1 - 8 (Cancelled)

9. (Previously Presented) A device comprising:

a semiconductor substrate;

a stacked cross point array formed over the semiconductor substrate, the stacked cross point array having at least two layers of memory cells, each successive layer of memory cells being formed over the previous layer of memory cells; and

drivers that are formed on the semiconductor substrate, the drivers being in electrical communication with the stacked cross point array;

wherein the stacked cross point array has at least two separate access times, the fastest of which is associated with the layer of memory cells closest to the semiconductor substrate;

wherein placement of the drivers contribute to the access time associated with the layer of memory cells closest to the semiconductor substrate being the fastest access time.

10. (Original) The device of claim 9, wherein:

the stacked cross point array has only two separate access times.

11. (Previously Presented) A device comprising:

a stacked cross point having

a first x-direction conductive array line layer;

a first memory plug layer having a first access time, and positioned on top of the first x-direction conductive array line layer;

a first y-direction conductive array line layer on top of the first memory plug layer;

a second memory plug layer having a second access time, and positioned on top of the first y-direction conductive array line layer; and

a second x-direction conductive array line layer on top of the second memory plug layer;

a first x-direction driver set in electrical communication with the first x-direction conductive array line layer;

a y-direction driver set in electrical communication with the first y-direction conductive array line layer; and

a second x-direction driver set in electrical communication with the first x-direction conductive array line layer;

wherein the first access time is faster than the second access time; and

wherein placement of the first and second x-direction drivers contribute to the first access time being faster than the second access time.

12. (Original) The device of claim 11, wherein:

the memory plug layers exhibit a non-linear resistive characteristic.

13. (Previously Presented) The device of claim 12, wherein:

the memory plugs include conductive metal oxides.

14. (Original) The device of claim 11, wherein:

the device is part of a re-writable memory.

15. (Previously Presented) The device of claim 9 wherein the memory cells are re-writable.

16. (Previously Presented) The device of claim 9 wherein the memory cells include conductive metal oxides.

17. (Previously Presented) The device of claim 11 wherein:

the first x-direction conductive array line layer includes a plurality of x-direction conductive array lines, each x-direction conductive array line having a middle and two ends along the x-direction;

the first x-direction driver includes a plurality of individual x-direction drivers, each individual x-direction driver connected to the middle of an x-direction conductive array line;

the plurality of x-direction conductive array lines includes an array cut, the array cut being where two contiguous x-direction conductive array lines are spaced further apart than other contiguous x-direction conductive array lines;

the first y-direction conductive array line layer includes a plurality of y-direction conductive array lines, each y-direction conductive array line having a middle and two ends along the y-direction;

the first y-direction driver includes a plurality of individual y-direction drivers, each individual y-direction driver connected to the middle of a y-direction conductive array line through the array cut.